AF RFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Darmawan	Attorney Docket No.: CREEP027/P02111
Application No.: 10/053,424	Examiner: Tran, Tan N.
Filed: November 2, 2001	Group: 2826
Title: SILICON ON INSULATOR DEVICE WITH IMPROVED HEAT REMOVAL (As amended)	Confirmation No.: 4303

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on October 14, 2004 in an envelope addressed to the Commissioner for Patents, Mail Stop Appeal Brief-Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Laura M. Dean

APPEAL BRIEF TRANSMITTAL
(37 CFR 192)

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is in furtherance of the Notice of Appeal filed in this case on January 13, 2004. This brief is transmitted in triplicate.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:
☐ $170.00 (Small Entity) ☐ $340.00 (Large Entity)*

*This is the second Appeal Brief in the Application

☐ Applicant(s) hereby petition for a _____ extension(s) of time to under 37 CFR 1.136.

If an additional extension of time is required, please consider this a petition therefor.

☐ An extension for months has already been secured and the fee paid therefor of $ is deducted from the total fee due for the total months of extension now requested.

☒ Because this is the second Appeal submitted for this application, Applicant(s) believe that no (additional) Appeal Brief Fee or Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an extension be granted and authorize the Commissioner to charge the required fees for an Appeal Brief and/or Extension of Time under 37 CFR 1.136 to Deposit Account No. 50-0388.

Total Fee Due:

Appeal Brief fee	$340.00 (2nd Appeal)
Extension Fee (if any)	$
Total Fee Due	$0.00

☒ Charge any additional fees or credit any overpayment to Deposit Account No. 500388, (Order No. CREEP027).

Respectfully submitted,
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE DARMAWAN

Application for Patent

Filed November 2, 2001

Serial No. 10/053,424

FOR:

SILICON ON INSULATOR DEVICE WITH IMPROVED HEAT REMOVAL (AS AMENDED)

APPEAL BRIEF

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Signed: _____
Laura M. Dean

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Attorneys for Applicant

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This is an appeal from the Office Action mailed September 16, 2004, finally rejecting claims 15 and 21-23 in the above-identified patent application. A copy of the claims on appeal are in the attached appendix.

I. REAL PARTY IN INTEREST

The real party in interest is Cree Microwave, Inc., by change of name from Ultra RF, Inc., of Sunnyvale, CA, assigned from Johan August Darmawan, inventor and applicant.

II. RELATED APPEALS AND INTERFERENCES

This is the third Final Rejection and the second appeal of a Final Rejection in the application, the first two final rejections having been withdrawn.

III. STATUS OF THE CLAIMS

Method claims 1-14 are being prosecuted in divisional patent application serial no. 10/327,479, now U.S. Patent No. 6,740,548 issued May 25, 2004, device claims 16-20 are cancelled and device claims 15 and 21-23 as amended remain in the application.

IV. STATUS OF AMENDMENTS

No amendment has been filed subsequent to this third final rejection.

V. SUMMARY OF INVENTION

The invention relates generally to silicon on insulator (SOI) semiconductor devices and manufacturing processing. As described in the background of the invention, reduced parasitic components can be achieved in semiconductor devices by fabrication of the devices in a silicon on insulator structure, such as silicon on sapphire and silicon on oxide insulator , including commercially available bonded silicon on insulator and implanted oxide (SIMOS). In such structures the supporting substrate is typically bonded to a heat sink for heat removal, which is particularly important for power transistor structures. Additionally, a ground plane can be provided by metallization on the substrate surface.

The claimed invention is directed to an SOI device having improved heat removal and with a simple structure which readily facilitates manufacture. With reference to Fig. 1D (copy as exhibit 2 in the appendix) in one embodiment a component such as a transistor 16 is fabricated in silicon layer 14 which is supported by substrate 10 with a silicon oxide layer 12 therebetween. A heat sink for component 16 comprises a metal layer or plug including refractory metal 20 and a metal layer 22. Metal layer 22 can be gold, copper, or aluminum, for example, which is compatible in semiconductor device and integrated circuit structures and manufacturing processes. The refractory metal 20 is optional in the structures.

An important feature of the invention is the provision of a single heat sink comprising metal 20, 22 in a recessed portion of substrate 10 in close proximity to component 16 and insulated therefrom by silicon oxide layer 12. Further, as shown in Fig. 1c, the recessed portion in substrate 10 is formed by a preferential etchant which etches substrate 10 and with silicon oxide layer 12 functioning as an etchant stop, thereby preventing over etching into silicon oxide layer 12 and silicon layer 14. This structure is simple and readily manufactured.

Thus, in accordance with the invention as defined by claim 15, a metal layer (plug) is formed in the portion of the substrate in which silicon has been removed by etching, the metal layer abutting the silicon oxide layer and providing heat removal from the component, the silicon oxide layer electrically insulating the metal layer from the semiconductor component. Claims 21-23 further define the metal layer.

VI. ISSUES

Claims 15 and 21-23 have been finally rejected under 35 USC 103(a) as being unpatentable over Lin U.S. Patent No. 6,483,147 in view of Buynowski U.S. Patent No. 6,190,985, the Examiner referring to the SOI substrate 40 and metal layer 52 shown in Lin Fig. 7 and silicon oxide layer 34 which insulates metal layer 14 in Buynoski Fig. 6.

The sole issue in this appeal is whether Lin can be modified by the teachings of Buynoski to suggest the invention as defined by claims 15 and 21-23.

VII. GROUPING OF CLAIMS

The claims are a single group for purposes of appeal.

VIII. ARGUMENT

THE SILICON ON INSULATOR (SOI) SEMICONDUCTOR DEVICE AS DEFINED BY CLAIM 15 IS NOT SUGGESTED BY LIN IN VIEW OF BUYNOSKI.

The basic distinction between the device as defined by claim 15 and the devices disclosed by Lin and Buynoski is straight forward.

Claim 15 recites:

> a) a semiconductor body including a silicon supporting substrate, a silicon oxide layer supported by the substrate, and a silicon layer overlying the silicon oxide layer,
>
> b) a semiconductor component formed in the silicon layer overlying a portion of the substrate in which silicon has been removed by etching, and
>
> c) **a metal layer in the portion of the substrate in which silicon has been removed by etching, the metal layer abutting the silicon oxide layer and providing heat removal from the component, the silicon oxide layer electrically insulating the metal layer from the semiconductor component.** (Emphasis added).

The recited metal layer for heat removal is compatible with semiconductor device fabrication and facilitates heat removal by being placed close to the semiconductor component but electrically insulated therefrom by abutting silicon oxide layer 12. Moreover, the device is simple in structure and readily manufactured.

Lin describes a backside metal contact to a SOI semiconductor device in which the contact comprises a conductive plug 38 that electrically contacts the semiconductor device 32 through a hole in silicon substrate layer 12 and insulation layer 34. Thus the contact is intended to be an electrical terminal of the device and necessarily physically and electrically contacts the device.

This is not the structure or function of the metal layer in the claimed invention where a silicon oxide layer electrically insulates the metal layer from the semiconductor component. While the invention leaves the insulating layer intact and thereby functions as an etch stop in etching the substrate, Lin intentionally removes the insulation layer so that the conductive plug 38 electrically and physically contacts the semiconductor device 32. This feature is specifically claimed by Lin, in particular reciting, "a conductive plug

through the silicon substrate layer and the insulation layer contacting the silicon device layer, wherein the conductive plug extends into the silicon device layer."

Buynoski discloses the use of two separate heat sinks in his SOI structure, namely the metal layer 14 which is deposited on a buried insulation layer 34 over the bulk silicon substrate 12 and optionally a separate heat sink, either 36 or 38, to the metal layer heat sink 14. See Figs. 4, 5 and 7 for the three embodiments of Buynoski in which only a single heat sink metal layer 14 is used in Fig. 4 and second heat sinks 36, 38 are provided to the single heat sink layer 14 as shown in Figs. 5 and 6.

Buynoski specifically describes the conductive plugs 36,38 as serving to facilitate transfer of heat away from metal base layer 14 with the heat removed via the conductive plugs dissipated in the bulk silicon layer. See column 4, lines 59-64.

In fact, the metal plugs 36,38 are not required in the Buynoski structure, as shown in Figs. 3 and 4 where the single heat sink, metal layer 14 is employed.

The Buynoski structure which employs a metal based layer 14 in the SOI structure is entirely different from and more complicated than the claimed silicon on insulator semiconductor device comprising a semiconductor body including a silicon supporting substrate, a silicon oxide layer supported by the substrate, and a silicon layer overlying the silicon oxide layer. A metal layer corresponding to Buynoski's layer 14 is not needed nor included.

Further, the claimed silicon on insulator semiconductor device has a single heat sink in the metal layer in the portion of the substrate in which silicon has been removed by etching with the metal layer abutting the silicon oxide layer and providing heat removal from the component. Buynoski utilizes metal layer 14 as the heat sink with, optionally, a metal plug 36 or 38 functioning as a second heat sink for heat sink metal layer 14.

Further, claim 15 specifies that the metal layer in the portion of the substrate in which silicon has been removed by etching abuts the silicon oxide layer electrically insulating the metal layer from the semiconductor component. In Buynoski, plug 38 does not abut the silicon oxide layer, as claimed, since plug 38 abuts and removes heat from metal heat sink layer 14. The metal heat sink layer 14 is unnecessary in the claimed invention.

It is respectfully noted that the present Office Action is the seventh substantive action on the application, including two earlier Final Rejections which have been

withdrawn and now this third final rejection. The previous rejections have been based on the Lin reference taken with Takahashi, Lin taken with Udrea, Lin taken with Armbrust, and now Lin taken with Buynoski. It is not seen that Buynoski is any more relevant than the previously cited prior art. Indeed, Buynoski appears to be less relevant in proposing a SOI device structure including two heat sinks (metal layer and metal plug) which complicates the manufacture and resulting structure of the Buynoski device when compared to the claimed silicon on insulator semiconductor device in which a single heat sink is provided by a metal layer in a portion of the substrate in which silicon has been removed by etching with the metal layer abutting the silicon oxide layer and providing heat removal from the component.

For the forgoing reasons, it is respectfully submitted that independent claim 15 and dependent claims 21-23 are neither shown nor suggested by Lin taken with Buynoski, singly or combined.

IX. CONCLUSION

The silicon on insulator semiconductor device as defined by claims 15 and 21-23 is neither shown nor suggested by Lin taken with Buynoski. The rejections of claims 15 and claims 21-23 under 35 USC 103(a) on Lin in view of Buynoski, should be reversed.

Respectfully Submitted,
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X. APPENDIX

CLAIMS ON APPEAL

Claims 1-14 (Withdrawn).

15. A silicon on insulator (SOI) semiconductor device comprising:

a) a semiconductor body including a silicon supporting substrate, a silicon oxide layer supported by the substrate, and a silicon layer overlying the silicon oxide layer,

b) a semiconductor component formed in the silicon layer overlying a portion of the substrate in which silicon has been removed by etching, and

c) a metal layer in the portion of the substrate in which silicon has been removed by etching, the metal layer abutting the silicon oxide layer and providing heat removal from the component, the silicon oxide layer electrically insulating the metal layer from the semiconductor component.

Claims 16-20 (Cancelled).

21. The semiconductor device and defined by claim 15, wherein the metal layer comprises a refractory metal.

22. The semiconductor device as defined by claim 21, wherein the metal layer comprises gold, aluminum, or copper over the refractory metal.

23. The semiconductor device as defined by claim 21, wherein the refractory metal comprises titanium tungsten.

FORMAL DRAWINGS

Formal Drawings are attached hereto.

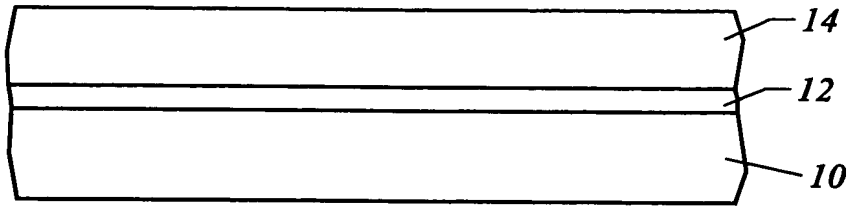

FIG. 1A

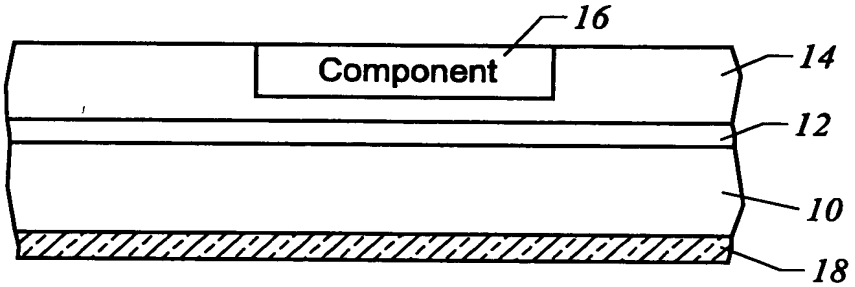

FIG. 1B

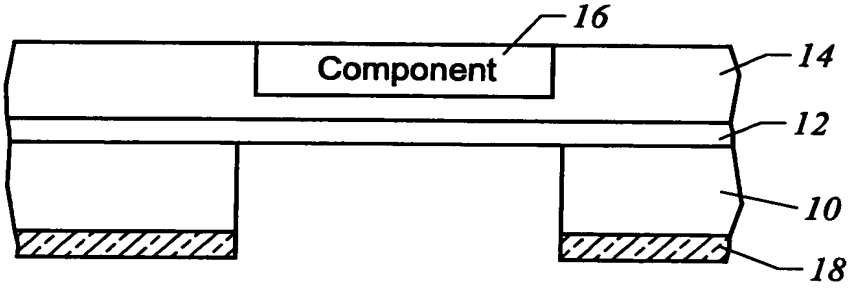

FIG. 1C

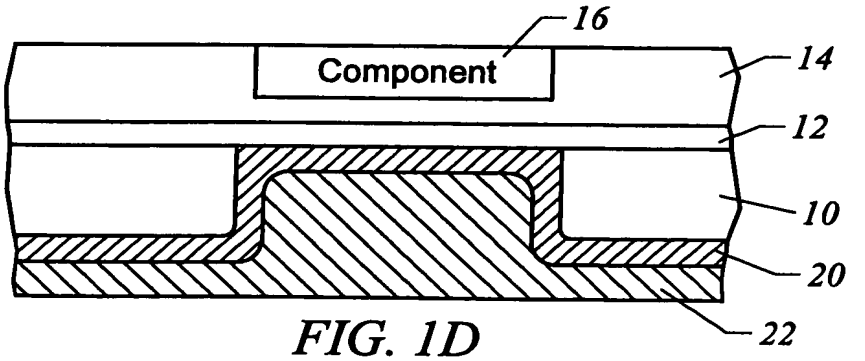

FIG. 1D

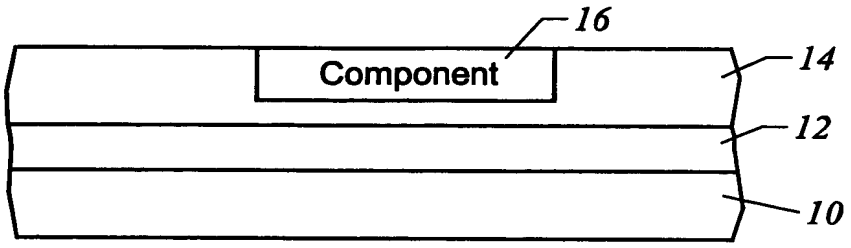

FIG. 2A

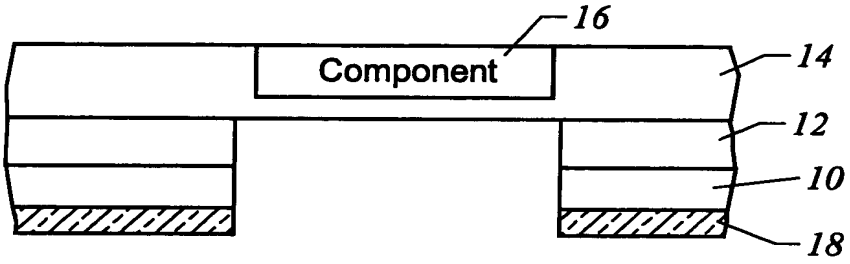

FIG. 2B

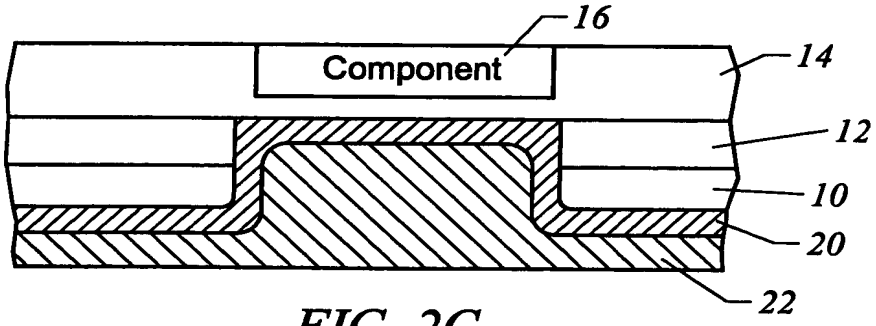

FIG. 2C

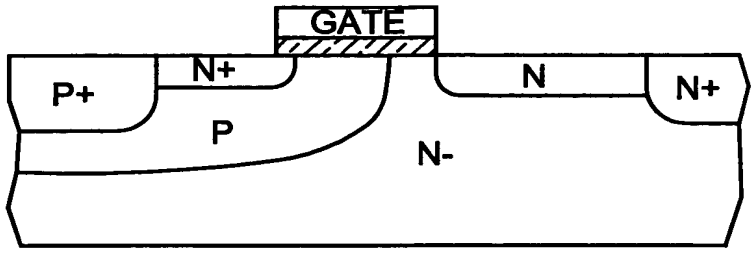

FIG. 3A

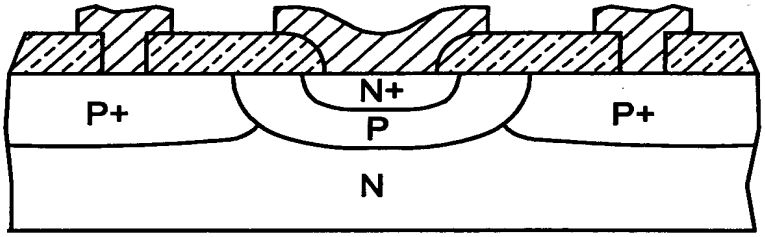

FIG. 3B

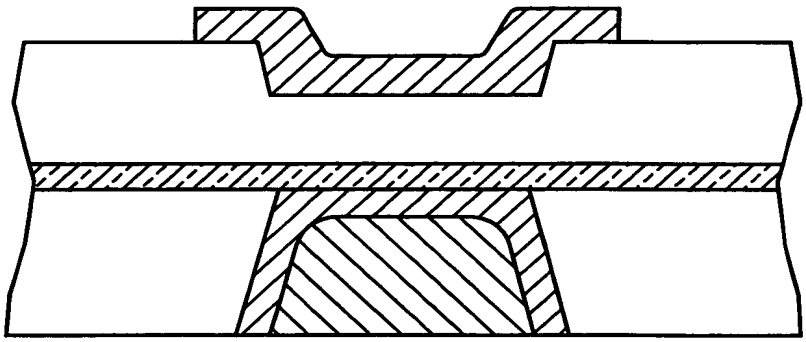

FIG. 3C